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Please find below and/or attached an Office communication concerning this application or proceeding.

Commissioner of Patents and Trademarks

Office Action Summary	Application No. 09/234,427	Applicant(s) Intrater et al.
	Examiner Pan	Art Unit 2183

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *three* MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136 (a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1) ☒ Responsive to communication(s) filed on *Jan 20, 1999*

2a) ☐ This action is **FINAL.** 2b) ☒ This action is non-final.

3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11; 453 O.G. 213.

Disposition of Claims

4) ☒ Claim(s) *2-8 and 11-44* is/are pending in the applica

4a) Of the above, claim(s) *1,9,10 (canceled claims)* is/are withdrawn from considera

5) ☒ Claim(s) *2-8 and 37-39* is/are allowed.

6) ☒ Claim(s) *1-17, 19-26, 28-35, 37, 38, and 40-44* is/are rejected.

7) ☒ Claim(s) *18, 27, and 36* is/are objected to.

8) ☐ Claims _____ are subject to restriction and/or election requirem

Application Papers

9) ☐ The specification is objected to by the Examiner.

10) ☐ The drawing(s) filed on _____ is/are objected to by the Examiner.

11) ☐ The proposed drawing correction filed on _____ is: a) ☐ approved b) ☐ disapproved.

12) ☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. § 119

13) ☐ Acknowledgement is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d).

a) ☐ All b) ☐ Some* c) ☐ None of:

1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

*See the attached detailed Office action for a list of the certified copies not received.

14) ☐ Acknowledgement is made of a claim for domestic priority under 35 U.S.C. § 119(e).

Attachment(s)

15) ☒ Notice of References Cited (PTO-892)

16) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)

17) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s). _____

18) ☒ Interview Summary (PTO-413) Paper No(s). *herewith*

19) ☐ Notice of Informal Patent Application (PTO-152)

20) ☐ Other:

1. Claim 2-8,11-44 are presented for examination. Claims 1,9,10 have been canceled. S.N. 08/317,783 is the application number for the surrendered patent 5,630,153.

2. Claims 11,20,29 are rejected under 35 U.S.C. 251 as being an improper recapture of broadened claimed subject matter surrendered in the application for the patent upon which the present reissue is based. See *Hester Industries, Inc.* v. *Stein, Inc.*, 142 F.3d 1472, 46 USPQ2d 1641 (Fed. Cir. 1998); *In re Clement,* 131 F.3d 1464, 45 USPQ2d 1161 (Fed. Cir. 1997); *Ball Corp.* v. *United States*, 729 F.2d 1429, 1436, 221 USPQ 289, 295 (Fed. Cir. 1984). A broadening aspect is present in the reissue which was not present in the application for patent. The record of the application for the patent shows that the broadening aspect (in the reissue) relates to subject matter that applicant previously surrendered during the prosecution of the application. Accordingly, the narrow scope of the claims in the patent was not an error within the meaning of 35 U.S.C. 251, and the broader scope surrendered in the application for the patent cannot be recaptured by the filing of the present reissue application.

3. As to reissue claims 11,20, applicant indicated in Paper #34 that claim 28 (claim 27 by applicant and corrected by Examiner as claim 28 in Paper 34, now claim 7 in the patent) included the combined features of canceled claim 5 which had previously been rejected under "103" as unpatentable over Davis et al. (4,991,169) in view of Doornink et al. (5,185,599) , and claim 6 objected ,respectively, as set forth in Paragraphs V and X in Paper # 31. The limitations of canceled claims 5,6 which were recited in the newly presented claim 28 in Paper # 34 was used to

obviate the rejection. The feature of the first bus (reissue claim 11 , line 2) is the broadening feature of "shared internal bus" (Patent claim 7, paragraph c), and "a memory connected to the first bus" (reissue claim 11, line 3) is the broadening feature of "a shared internal memory array connected to the shared internal bus" (patent claim 7, paragraph d).

4. The omitted features are :

a) the selection of the sequence of DSP instructions for execution by the digital signal execution unit from set of DSP instructions and that perform general purpose processing tasks by executing the general purpose instructions (see claim 7, line 14);

b)transferring both data and instructions and to which both the digital signal execution unit and the general purpose processor are connected (claim 7, lines 16-18);

c)shared memory array accessible by the digital signal execution unit via the internal input and output port for transferring operand utilizable by digital signal execution unit between the shared internal memory array and the digital execution unit the shared internal bus and such that the shared internal memory is accessible by general purpose processor via the internal input and output port for transferring the general purpose instructions and the selected data between the shared internal memory and the general purpose processor on the internal bus (See claim 7, lines 21-33);

c)the shared interface unit recited in claim 7, lines 34-44).

5. Although the reissue claim 11 presented additional feature of starting execution of an instruction in response to the general purpose processor loading information into a register (see

reissue claim 11, line 8-10, see also identification of the instruction in claim 20, last line), these features are not related to the prior art rejection and not related to the subject matter surrendered in the original application. Therefore, impermissible recapture of the subject matter exist.

6. As to claim 29, applicant indicated in Paper #34 that claim 29 (claim 28 by applicant and corrected by Examiner as claim 29 in Paper 34, now claim 9 in the patent) included a the combined features of canceled claim 5 which had previously been rejected under "103" as unpatentable over Davis et al. (4,991,169) in view of Doornink et al. (5,185,599) , and claim 20 objected ,respectively, as set forth in Paragraphs V and X in Paper # 31. The limitations of canceled claims 5,20 which were recited in the newly presented claim 29 in Paper # 34 was used to obviate the rejection. The feature of the first bus (reissue claim 29 , line 2) is the broadening feature of "shared internal bu" (Patent claim 9, paragraph c), and "a memory connected to the first bus" (reissue claim 29, line 3) is the broadening feature of "a shared internal memory array connected to the shared internal bus" (patent claim 29, paragraph d).

7. The omitted features are :

a) the selection of the sequence of DSP instructions for execution by the digital signal execution unit from set of DSP instructions and that perform general purpose processing tasks by executing the general purpose instructions (see patent claim 9, paragraph b);

b)transferring both data and instructions and to which both the digital signal execution unit and the general purpose processor are connected (claim 9, paragraph c);

c)shared memory array accessible by the digital signal execution unit via the internal input and output port for transferring operand utilizable by digital signal execution unit between the shared internal memory array and the digital execution unit the shared internal bus and such that the shared internal memory is accessible by general purpose processor via the internal input and output port for transferring the general purpose instructions and the selected data between the shared internal memory and the general purpose processor on the internal bus (See claim 9, paragraph d);

c)the shared interface unit recited in claim 9, lines 20-23);

d)the retrieval of the operands from the shared memory array via shared internal bus for use by the digital execution unit in executing the selected sequence of DSP instructions (patent claim 9, lines 20-24).

8. Although the reissue claim 29 presented additional feature of "executing an instruction in response to GPP loading information into the register" (see claim 29, line 8-9), this feature is not related to the prior art rejection and not related to the subject matter surrendered in the original application. Therefore, impermissible recapture of the subject matter exist.

9. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are

such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 11-17,19,20-26,28,29,30-35,40-44 are rejected under 35 U.S.C. 103(a) as being unpatentable over Parruck et al. (4,799,144) In view of Akagi et al. (4,467,414).

10. Parruck disclosed a data processing system (e.g. see overview in fig.1, and the DSP in fig.6) comprising at least :

a)a first bus (fig.1 [26]);

b)a memory [18] connected to the first bus ;

c)a general purpose processor [on board processor] connecting to the first bus (see fig.1[14]);

d)a digital signal processor [16] connected to the first bus, the dsp having a memory [RAM] and starting execution of instructions in response to the general purpose processor [14] loading information into the memory [RAM] (e.g. see col.6, lines 49-60).

11. As to claims 11, 12,19, Parruck did not clearly show that his general purpose processor [14] was loading operands into the memory [18] as recited in applicant's claim 11, line 5. Instead, Parruck taught the loading of necessary information into the memory [18] for running particular application program (e.g. see col.6, lines 42-45). However, Akagi disclosed a system for loading operands into a memory necessary for operation (e.g. see col2, lines 15-22). It would have been obvious to one of ordinary skill in the art to use Akagi in Parruck for loading operands into a memory as claimed because the use of Akagi could enhance the memory control

of Parruck to store particular type of operands at memory access level , and Parruck did show the need for loading the operands into the memory by disclosing the loading of the necessary information into the memory to run a particular application program (e.g. see col.6, lines 50-53), as already known, opcodes and operands were building elements of programming instructions which were necessary information for running application, and Akagi could be easily implemented into Parruck by modifying the format of instruction operands of Akagi such that it would be recognizable by the access control of the general purpose processor of Parruck, such as read/write operations. Therefore, for the reasons discussed above, it would have bee obvious to one of ordinary skill in the art to use Akagi in Parruck for loading operands into the memory as claimed.

12. As to claims 13, Parruck did not explicitly show the identification of the instruction as claimed (see claims 13, line 3, claim 20, line 11, claim 22), However, Parruck taught that any new application program could be easily implemented into his system by only introducing a new software (e.g. see col.5, lines 29-33). Therefore, Parruck must have a control to distinguish and identify the new program (the instructions) from the already existed program instructions. Otherwise, the introduction of new software would not be possible. And , for this reason it would have been obvious to one of ordinary skill in the art to identify instructions in a memory system , such as the Parruck's, as claimed (see the reason just set forth above).

13. As to claims 14, Parruck also included a second bus (see fig.1 [17]).

14. As to claims 15, Parruck's general purpose processor had to be placed in wait state because only one of the general purpose [14] and dsp [16] could interface directly to the switch memory [18] (e.g. see col.3, lines 16-23).

15. As to claim 16,17, Parruck's general processor [14] also read status after the completion of the DSP (e.g. see the resetting , stopping or running of the dsp by the control bit of general processor [14] in col.3, lines 5-15).

16. As to claims 20,21,28, Parruck did not clearly show that his general purpose processor [14] was loading operands into the memory [18] as recited in applicant's claim 20, line 5. Instead, Parruck taught the loading of necessary information into the memory [18] for running particular application program (e.g. see col.6, lines 42-45). However, Akagi disclosed a system for loading operands into a memory necessary for operation (e.g. see col2, lines 15-22). It would have been obvious to one of ordinary skill in the art to use Akagi in Parruck for loading operands into a memory as claimed because the use of Akagi could enhance the memory control of Parruck to store particular type of operands at memory access level , and Parruck did show the need for loading the operands into the memory by disclosing the loading of the necessary information into the memory to run a particular application program (e.g. see col.6, lines 50-53), as already known, opcodes and operands were building elements of programming instructions which were necessary information for running application, and Akagi could be easily implemented into Parruck by modifying the format of instruction operands of Akagi such that it

would be recognizable by the access control of the general purpose processor of Parruck, such as read/write operations. Therefore, for the reasons discussed above, it would have bee obvious to one of ordinary skill in the art to use Akagi in Parruck for loading operands into the memory as claimed.

17. As to claims 20, 22, Parruck did not explicitly show the identification of the instruction as claimed (see claim 20, line 11, claim 22), However, Parruck taught that any new application program could be easily implemented into his system by only introducing a new software (e.g. see col.5, lines 29-33). Therefore, Parruck must have a control to distinguish and identify the new program (the instructions) from the already existed program instructions. Otherwise, the introduction of new software would not be possible. And , for this reason it would have been obvious to one of ordinary skill in the art to identify instructions in a memory system , such as the Parruck's, as claimed (see the reason just set forth above).

18. As to claim 23, Parruck also included a second bus (see fig.1 [17]).

19. As to claim 24, Parruck's general purpose processor had to be placed in wait state because only one of the general purpose [14] and dsp [16] could interface directly to the switch memory [18] (e.g. see col.3, lines 16-23).

20. As to claims 25,26, Parruck's general processor [14] also read status after the completion of the DSP (e.g. see the resetting , stopping or running of the dsp by the control bit of general processor [14] in col.3, lines 5-15).

21. As to claims 29,30, Parruck did not clearly show that his general purpose processor [14] was loading operands into the memory [18] (claim 29, line 5) and retrieving the operands (claim 29, line 10). Instead, Parruck taught the loading of necessary information into the memory [18] for running particular application program (e.g. see col.6, lines 42-45). However, Akagi disclosed a system for loading operands into a memory necessary for operation (e.g. see col.2, lines 15-22), and retrieving the operand (see the reading out request of the operand in col.5, lines 30-37, col.8, lines 57-60, col.10, lines 15-21). It would have been obvious to one of ordinary skill in the art to use Akagi in Parruck for loading operands into a memory, and retrieving the operand as claimed because the use of Akagi could enhance the memory control of Parruck to store particular type of operands at desired access level , and Parruck did show the need for loading the operands into the memory and retrieving the operands by disclosing the loading of the necessary information into the memory to run a particular application program (e.g. see col.6, lines 50-53), as already known, opcodes and operands were building elements of programming instructions which were necessary information for running application, and Akagi could be easily implemented into Parruck by modifying the format of instruction operands of Akagi such that it would be recognizable by the access control of the general purpose processor of Parruck, such as read/write operations. Therefore, for the reasons discussed above, it would have bee obvious to one of ordinary skill in the art to use Akagi in Parruck for loading operands into the memory as claimed.

22. As to claim 31, Parruck did not explicitly show the identification of the instruction as claimed (see claim 20, line 11, claim 22), However, Parruck taught that any new application program could be easily implemented into his system by only introducing a new software (e.g. see col.5, lines 29-33). Therefore, Parruck must have a control to distinguish and identify the new program (the instructions) from the already existed program instructions. Otherwise, the introduction of new software would not be possible. And , for this reason it would have been obvious to one of ordinary skill in the art to identify instructions in a memory system , such as the Parruck's, as claimed (see the reason just set forth above).

23. As to claim 32, Parruck also included a second bus (see fig.1 [17]).

24. As to claim 33, Parruck's general purpose processor had to be placed in wait state because only one of the general purpose [14] and dsp [16] could interface directly to the switch memory [18] at a time (e.g. see col.3, lines 16-23).

25. As to claims 34,35, Parruck's general processor [14] also read status after the completion of the DSP (e.g. see the resetting , stopping or running of the dsp by the control bit of general processor [14] in col.3, lines 5-15).

26. As to claims 40,41, Parruck disclosed a system (see fig.1) comprising at least :

a)a first data bus [88];

b)a second data bus [17];

c)a memory [18] connected to the first data bus and the second data bus;

d)a general purpose processor [14] connected to the first data bus (see fig.1), the DSP executing instructions under the control of general purpose processor [14 (see the restart, stopping nas running by general purpose processor in col.3, lines 7-13).

27. Parruck did not clearly show that his general purpose processor [14] was loading operands into the memory [18] (claim 40, line 7), and retrieving the operands (claim 40, line 2 from the bottom of the claim). Instead, Parruck taught the loading of necessary information into the memory [18] for running particular application program (e.g. see col.6, lines 42-45). However, Akagi disclosed a system for loading operands into a memory necessary for operation (e.g. see col.2, lines 15-22), and retrieving the operand (see the reading out request of the operand in col.5, lines 30-37, col.8, lines 57-60, col.10, lines 15-21). It would have been obvious to one of ordinary skill in the art to use Akagi in Parruck for loading operands into a memory, and retrieving the operand as claimed because the use of Akagi could enhance the memory control of Parruck to store particular type of operands at a desired access level , and Parruck did show the need for loading the operands into the memory and retrieving the operands by disclosing the loading of the necessary information into the memory to run a particular application program (e.g. see col.6, lines 50-53), as already known, opcodes and operands were building elements of programming instructions which were necessary information for running application, and Akagi could be easily implemented into Parruck by modifying the format of instruction operands of Akagi such that it would be recognizable by the access control of the general purpose processor of Parruck, such as the read/write attributes. Therefore, for the reasons discussed above, it

would have bee obvious to one of ordinary skill in the art to use Akagi in Parruck for loading operands into the memory as claimed.

28. Parruck did not explicitly show the identification of the instruction as claimed (see claim 40, line 11), However, Parruck taught that any new application program could be easily implemented into his system by only introducing a new software (e.g. see col.5, lines 29-33). Therefore, Parruck must have a control to distinguish and identify the new program (the instructions) from the already existed program instructions. Otherwise, the introduction of new software would not be possible. And , for this reason it would have been obvious to one of ordinary skill in the art to identify instructions in a memory system , such as the Parruck's, as claimed (see the reason just set forth above).

29. Parruck did not specifically show his first data bus connected to the dsp as claimed (see claim 40, line 10). However, the function of the first data bus being connected to the DSP has not been recited in the claim. Therefore , this connection (first bus connected with the DSP) is assumed to have no affect on the functioning of the claimed invention , and therefore, it has no patentable weight. The Examiner will reconsider this connection when applicant responds in the claim with a clear function of the connection.

30. As to claim 42, Parruck's general purpose processor had to be placed in wait state because only one of the general purpose [14] and dsp [16] could interface directly to the switch memory [18] at a time (e.g. see col.3, lines 16-23).

31. As to claim 43, Parruck's general processor [14] also read status after the completion of the DSP (e.g. see the resetting , stopping or running of the dsp by the control bit of general processor [14] in col.3, lines 5-15).

32. As to claim 44, Parruck also included :

a)a bus interface unit [30][12] connected to the first data bus (see fig.1 [30][12]);

b)a third data bus connected to the bus interface (see the connection bus from [12] to host in fig.1).

33. Claims 18,27,36 objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

34. Claims 2-8,37-39 are allowable over the art of record.

35. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Daniel Pan whose telephone number is (703) 305 9696. The examiner can normally be reached on M-F from 8:00 AM to 4:30 PM.

36. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Chan, can be reached on (703) 305 9712. The fax phone number for the organization where this application or proceeding is assigned is (703) 305 3718.

37. Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 305 3900.

DANIEL H. PAN
PRIMARY EXAMINER
GROUP